REMARKS

SUMMARY

Reconsideration of the application is respectfully requested.

Claims 1-28 are in the application.

Applicant appreciatively acknowledges the Examiner's consideration and acceptance of the information disclosure statement (IDS) received on August 23, 2004.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102

In "Claim Rejections – 35 USC § 102," item 3 on page 3 of the above-identified Office Action, claims 1-6 and 8-12 have been rejected as being fully anticipated by U.S. Patent No. 4,716,323 to *Wada, et al.* (hereinafter "Wada") under 35 U.S.C. § 102(e). Applicant respectfully traverses.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a detector circuit including:

a first device **coupled to input and output terminals**, to pull the output terminal to a first output voltage when a supply voltage below a supply threshold is applied to the input terminal, ***and*** the first device being configured to have ***no substantial change in current consumption after the supply voltage*** applied to the input terminal has ***exceeded the supply threshold***; and

a second device **coupled to the input, ground and output terminals**, to pull the output terminal to a second output voltage when the supply voltage applied to the input terminal exceeds the supply threshold.

Similar claim language may also be found in independent Claim 8 and Claim 12.

The Wada reference discloses a circuit for detecting power voltage drops. More specifically, Fig. 1 of Wada discloses the use of a pair of enhancement type MOS transistors Q1 and Q3 and a pair of depletion type MOS transistors Q2 and Q4. The voltage dividing circuit in Fig. 2 of Wada uses a resistor R and an n-channel enhancement MOS Q5. Fig. 2 of Wada also includes a switching portion of the circuit that uses both a p-channel (Q6) and an n-channel (Q7) MOS transistor, but they are both enhancement type transistors.

The transistors Q1 and Q2 of Wada form a voltage dividing circuit between the VDD terminal and the ground terminal. Q1 and Q2 in Wada do not show "***no change in current consumption after the supply voltage ...exceeded the supply threshold***" as recited in claim 1 of the instant application. Rather because Q1 of Wada is an enhancement n-channel MOS device, the combination of Q1 and Q2 in Wada will continue to increase current consumption even after the supply threshold is exceeded.

As previously indicated, the voltage dividing circuit in Fig. 2 of Wada uses a resistor R and an n-channel enhancement MOS Q5. Similar resistor based dividing configurations are shown in Figs. 6 and 8-11 of Wada. Clearly, the resistor based dividing configurations of Wada depicted in Figs. 2, 6, and 8-12 do not show "***no change in current consumption after the supply voltage ...exceeded the supply threshold***" as recited in claim 1 of the instant application. Similar language is found in independent claims 8 and 12.

To anticipate the instant application Wada must teach EVERY element of the claims, specifically "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, not only must the claim be expressly or inherently described, but "**The identical invention** must be shown **in as complete detail as is contained in the ... claim**." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)(emphasis added). In the instant case, Wada uses enhancement transistors in one embodiment (Fig. 1) and a resistor (Fig. 2) in another embodiment instead of the depletion transistor shown in Figure 2 of the instant application, which helps the detector circuit to exhibit "***no change in current consumption after the supply voltage ...exceeded the supply threshold***" as recited in claim 1 of the instant application.

Clearly, Wada does not show, teach, or suggest a "detector circuit" configuration with the **identical invention** (*e.g.*, to minimize substantial change in current consumption in the detector circuit), nor does Wada show the detector circuit **in as complete detail as is contained in the ... claim** where the detector circuit exhibits "no substantial change in current consumption" as recited in claims 1, 8, and 12 of the instant application. More specifically, Wada does not teach or suggest using a detector circuit with"**a first device coupled to the input and output terminals** to pull the output terminal to a first threshold when a supply voltage below a supply threshold is applied to the input terminal ... configured to have **no substantial change in current consumption after the supply voltage ... exceeded the supply threshold**" AND a switching circuit with "**a second device coupled to the input, ground, and output terminals** to pull the output terminal to a second output voltage when the supply voltage...exceeds the supply threshold." as recited in claims 1 of the instant application.

In view of the foregoing, the Examiner is requested to withdraw the rejections under 35 U.S.C. § 102(e) in item3 "Claim Rejections – 35 USC § 102" on page 3 of the above-identified office action and issue a Notice of Allowance.

Applicant respectfully notes that although the Office Action Summary indicates claims 1-28 are rejected, there is no specific rejection of claim 7. Claim 7 is mentioned within the range of claims 1-12 in item 5 on page 3 of the office action, however, a specific rejection is never provided. Applicant respectfully requests further clarification regarding the indicated rejection in accordance with the Examiner's duty under 37 CFR § 1.104(c)(2), which indicates that "In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references."

MPEP 706 clarifies that "The goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity." In the instant case, there has been no clearly articulated rejection of claim 7. In fact, applicant has previously demonstrated how Wada actually lacks the component (Wada discloses enhancement NMOS and/or resistor) mentioned in claim 7, specifically, a "first device ...

depletion NMOS device" entirely. Claim 7 indicates that the detector circuit described in claim 1 includes:

> the first device comprises **a depletion NMOS** device with a drain of the depletion NMOS device coupled to the input terminal, and a source of the depletion NMOS device coupled to a gate of the depletion NMOS device and the output terminal; and
>
> the second device comprises a NMOS device with a drain of the NMOS device coupled to the output terminal, a gate of the NMOS device coupled to the input terminal, and a source of the NMOS device coupled to the ground terminal.

Thus, in light of Applicant's comments above it is believed that claim 7 is also allowable. In view of the foregoing, the Examiner is requested to either withdraw the rejections under 35 U.S.C. § 102(e) in "Office Action Summary" and issue a Notice of Allowance or to issue another non-final Office Action clearly articulating the rejection of claim 7.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

In "Claim Rejections – 35 USC § 103," item 5 on page 3 of the above-identified Office Action, claims 13-28 have been rejected as being obvious over Wada in view of U.S. Patent No. 6,943,592 to *Degoirat, et al.* (hereinafter "Degoirat") under 35 U.S.C. § 103(a).

As previously indicated, the claims of the instant application are patentable over Wada for at least the reasons provided above. While the rejection to the combination of Wada and Degoirat has been noted, it is respectfully believed that Degoirat does not overcome the deficiencies previously attributed to Wada. As such, it is believed that the claims were patentable over the combination of Wada and Degoirat in their original form and, therefore, the claims have not been amended to overcome the references.

The Degoirat reference discloses a detector of supply voltage range in an integrated circuit. For example, the Degoirat detector is designed to detect the crossing of low levels of supply voltage. A first arm of the Degoirat detector defines a first reference voltage and a second arm defines a second reference voltage. The first arm of Degoirat includes a resistive

divider bridge and the second arm of Degoirat includes a resistor series-connected with a native P type MOS transistor.

Thus, Degoirat also uses at least one resistor in various embodiments (Figs. 4, 5, and 7 of Degoirat) instead of the configuration using a depletion transistor as shown in Figure 2 of the instant application, which helps the detector circuit of the instant application to "***consume substantially a same amount of current when the supply voltage is below the supply threshold...***" and when the supply threshold is above and/or exceeds the supply threshold as recited in claims 17 and 21 of the instant application.

Clearly, the combination of Wada and Degoirat does not teach or suggest a system and/or method of operation with at least one device configured to "***consume substantially a same amount of current when the supply voltage is below the supply threshold, and whenthe supply voltage exceeds the supply threshold***" as recited in claims 17 and 21 of the instant application.

In view of the foregoing, the Examiner is requested to withdraw the rejections under 35 U.S.C. § 103(a) in item 5 "Claim Rejections – 35 USC § 103" on page 3 of the above-identified office action and issue a Notice of Allowance.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 8, 12, 17, or 21. Claims 1, 8, 12, 17, and 21 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 8, 12, 17, or 21.

In the event the Examiner should still find any of the remaining claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith. If any further extension of time is required, petition

for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Schwabe, Williamson and Wyatt, P.C., No. 50-0393.

CONCLUSION

In view of the foregoing, reconsideration and allowance of claims 1-28 are solicited. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (206) 407-1509. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge the Deposit Account of Schwabe, Williamson and Wyatt, P.C., No. 50-0393.

Respectfully submitted,
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